REMARKS

The Office Action of 05/30/2006 has been carefully considered. In response thereto, the claims have been amended as set forth above. Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1 and 3 were rejected as being anticipated by Yamada; claims 5-7 were rejected as being unpatentable over the same. Claims 507 were rejected as being unpatentable over Yamada in view of Keating. Claims 4, 8 and 9 were rejected as being unpatentable over Yamada in view of Shinhara. Claim 2 was rejected as being unpatentable over Yamada in view of Bauer. Claims 1 was also rejected as being anticipated by Keating.

Claim 1 has been amended to incorporate the features of claim 3, which has been canceled. The rejection of claim 3 stated in part:

> Regarding claim 3, Yamada teaches the RAM can be of a synchronous type, in which case the read operation would be performed in a first phase of a control or timing signal, and a write operation would be performed in a second phase of a control or timing signal (column 5, lines 59-68).

This rejection is respectfully traversed.

Yamada's teachings concerning a "RAM of a synchronization type" and a "RAM of a non-sychronization type" are made clear in col. 5, line 59 to col. 6, line 10. These teachings merely concern so-called set-up and hold times. They do not imply anything about a first phase of a control signal, a second phase of a control signal, etc. Accordingly, amended claim 1 is believed to patentably define over the cited references.

Withdrawal of the rejection and allowance of claims 1 and 2-9 is respectfully requested.

Respectfully submitted,

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